SYED RAQUEED BIN ALVEE

Dhaka, Bangladesh

raqueed@outlook.com | +8801620869115

LinkedIn Profile

Summary

Embedded Firmware Engineer with 4+ years of experience in Board Support Package (BSP) development, device driver development, and real-time firmware for ARM-based microcontrollers and SoC platforms. Extensive hands-on experience building device drivers from the ground up for STM32 and Silicon Labs platforms, including DMA controller implementation, clock tree configuration, PLL settings, and power domain management. Proficient in C/C++ with deep expertise in low-level embedded software design, hardware-software integration, and firmware debugging using JTAG/SWD tools.

Experienced in developing firmware across multiple layers of the embedded software stack including bootloaders, hardware abstraction layers, peripheral device drivers (CAN, UART, SPI, I2C), DMA controllers, interrupt handling, clock management, power management, and multi-threaded RTOS applications. Proven ability to collaborate with hardware engineers to ensure firmware-hardware compatibility and support board bring-up activities.

Core Skills

- **BSP & Device Driver Development:** Board Support Package (BSP) development, device driver development from the ground up, DMA controller implementation, hardware abstraction layers (HAL), bootloader development, board bring-up, firmware-hardware integration
- **Embedded Firmware & Low-Level Programming:** C, C++, ARM Cortex-M (STM32, Silicon Labs), bare-metal firmware, interrupt service routines, memory management, register-level programming
- **Real-Time Operating Systems:** FreeRTOS, real-time task scheduling, multi-threaded programming, RTOS primitives (semaphores, mutexes, queues), inter-task communication, priority-based scheduling
- **Peripheral Interfaces & Device Drivers:** CAN bus, UART, SPI, I2C, ADC, GPIO, PWM, timers, DMA-based peripheral drivers, interrupt-driven I/O, BLE communication stacks, cellular modem drivers, GNSS interfaces
- **SoC Architecture & Hardware Understanding:** ARM Cortex-M architecture, memory subsystems (cache, RAM, Flash), interrupt controllers (NVIC), DMA controllers, clock trees and PLL configuration, peripheral clock enables, power management units, power domain control, bus architectures (AHB, APB)
- **Clock & Power Management:** Clock tree configuration, PLL settings and tuning, peripheral clock management, power domain control (turning peripherals on/off), low-power state transitions (sleep, deep sleep, standby modes), clock gating, wake-up interrupt handling
- **Debugging & Development Tools:** JTAG/SWD debuggers (ST-Link, J-Link), stop-mode debugging, GNU ARM toolchain, GCC, GDB, logic analyzers, oscilloscopes, UART console debugging, profiling tools, static analysis
- **Software Development Practices:** Git version control, CI/CD automation (Jenkins), unit testing, code coverage analysis, code reviews, coding standards, technical documentation

- **Communication Protocols:** MQTT, HTTPS, TLS/SSL, TCP/IP, UDP, JSON data formats, AT command protocols, multi-node network architectures

Work Experience

Milwaukee Tool | Platform IoT | Chicago, USA

Embedded System Engineer II | Jan 2024 – March 2025

- Developed Board Support Packages (BSP) and device drivers for ARM Cortex-M based platforms (STM32, Silicon Labs) integrating multiple hardware subsystems including CAN bus, UART, SPI, I2C, BLE radios, cellular modems, and GNSS receivers.
- Built peripheral device drivers from the ground up including UART drivers, SPI drivers, I2C drivers, CAN bus drivers, ADC drivers, and GPIO control modules. Implemented DMA controllers for efficient memory-to-peripheral and peripheral-to-memory data transfers, supporting both single-transfer and circular buffer modes with interrupt-based completion handling.
- Configured clock trees, PLL settings, and peripheral clock enables for STM32 and Silicon Labs platforms, optimizing system clock frequencies, peripheral clock ratios, and power-performance trade-offs for real-time embedded applications.
- Implemented power domain management firmware including peripheral power-on/power-off sequences, low-power state transitions (sleep, deep sleep, standby modes), clock gating mechanisms, and wake-up interrupt handlers, achieving significant reductions in active and standby power consumption.
- Designed and implemented hardware abstraction layers (HAL) enabling firmware portability across different STM32 and Silicon Labs platform variants, abstracting hardware-specific register access, DMA configurations, and peripheral initialization sequences.
- Debugged complex firmware-hardware integration issues using JTAG/SWD debuggers (ST-Link, J-Link), stop-mode debugging, logic analyzers, and oscilloscopes to validate signal timing, protocol compliance, DMA transfer sequences, and hardware behavior.
- Collaborated with hardware engineers across multiple sites to support board bring-up activities, validate hardware designs, debug hardware-software compatibility issues, and provide firmware requirements for new platform variants.
- Performed firmware performance profiling and optimization using profiling tools and static analysis, optimizing memory footprint, execution time, DMA transfer efficiency, and interrupt latency for real-time embedded systems.

Embedded System Engineer I | Jun 2022 – Dec 2023

- Developed device drivers and BSP components for STM32 and Silicon Labs microcontrollers including peripheral initialization routines, interrupt service routines, DMA controller configuration, and register-level hardware control.
- Implemented DMA controllers for UART, SPI, I2C, and ADC peripherals, configuring DMA channels, stream priorities, data transfer modes (normal, circular), memory/peripheral increment settings, and DMA interrupt handlers for transfer completion and error handling.
- Configured peripheral clocks and clock trees on STM32 platforms, setting up system clock sources (HSI, HSE, PLL), PLL multipliers and dividers, AHB/APB prescalers, and peripheral clock enables for optimal performance and power efficiency.

- Implemented FreeRTOS-based multi-threaded firmware architecture including real-time task scheduling, inter-task communication using RTOS primitives (semaphores, mutexes, message queues), and interrupt-to-task synchronization mechanisms.
- Built firmware for BLE communication stacks, cellular modem AT command interfaces (UART-based), GNSS data parsers, watchdog timer drivers, and power management subsystems including low-power mode transitions and peripheral power control.
- Debugged embedded firmware using JTAG/SWD debuggers (ST-Link, J-Link), UART console logging, and logic analyzers to troubleshoot driver issues, DMA transfer problems, clock configuration errors, and hardware interface failures.
- Developed automated unit tests and firmware validation frameworks using Python and PyTest, integrated with Jenkins CI/CD pipelines for continuous firmware testing and regression validation.
- Participated in code reviews, maintained coding standards, and contributed to firmware documentation including driver API specifications, BSP integration guides, and hardware interface documentation.
- Used Git version control and GNU ARM toolchain (GCC, GDB) for embedded firmware development, compilation, and debugging on ARM Cortex-M platforms.

Texas A&M University – Kingsville | Texas, USA

Graduate Research Assistant | May 2021 – Jun 2022

- Developed embedded system validation frameworks and Hardware-in-the-Loop (HIL) testbeds for real-time cyber-physical systems, enabling system-level firmware validation under simulated operational scenarios.
- Designed and implemented machine learning pipelines for anomaly detection in embedded control systems, including data acquisition from embedded sensors, feature extraction, model training, and validation workflows.
- Collaborated with research teams to publish findings on embedded systems security and validation methodologies (IEEE conferences, 86+ citations).

Graduate Teaching Assistant | Jan 2021 – May 2021

- Designed and taught laboratory exercises for Digital Signal Processing (DSP) courses, covering embedded signal processing algorithms, filtering, and real-time analysis.
- Guided students in implementing DSP algorithms in MATLAB, emphasizing practical understanding of signal processing techniques for embedded communication systems.

Education

Texas A&M University – Kingsville – Kingsville, TX

Master of Science in Electrical Engineering | *Graduated 2022*

Thesis: Study on Artificial Intelligence-Based Ransomware Detection for Digital Substations

American International University – Bangladesh (AIUB) – Dhaka, Bangladesh

Bachelor of Science in Electrical and Electronic Engineering | *Graduated 2020*

Thesis: On-body humidity sensing antenna with polyimide for BAN applications over 5G networks

Project Highlights

BSP Development for Multi-Subsystem SoC Platform:

Developed complete Board Support Package for ARM Cortex-M based embedded platform integrating CAN bus controller, BLE radio, cellular modem (LTE-M/NB-IoT), and GNSS receiver. Built peripheral device drivers from the ground up for UART, SPI, I2C, CAN, ADC, and GPIO interfaces. Implemented DMA controllers for efficient data movement between peripherals and memory, supporting both polling and interrupt-driven operation modes. Configured clock trees, PLL settings, and peripheral clock enables. Designed hardware abstraction layers, bootloader initialization sequences, and power domain management for low-power operation.

Technologies: Embedded C/C++, ARM Cortex-M, STM32, BSP development, device drivers (UART, SPI, I2C, CAN, ADC), DMA controllers, clock tree configuration, PLL settings, HAL, bootloader, JTAG/SWD debugging

DMA Controller Implementation & Clock Tree Configuration:

Implemented DMA controllers for STM32 and Silicon Labs platforms, configuring DMA channels for UART, SPI, I2C, and ADC peripherals. Developed DMA transfer modes including memory-to-peripheral, peripheral-to-memory, and memory-to-memory operations with support for single-shot and circular buffer modes. Configured clock trees including system clock sources (HSI, HSE, PLL), PLL multiplier/divider ratios, AHB/APB bus prescalers, and peripheral clock enables. Optimized clock configurations for performance and power trade-offs, achieving target system frequencies while minimizing power consumption.

Technologies: STM32, Silicon Labs, DMA controllers, clock tree configuration, PLL settings, peripheral clock management, embedded C

Power Domain Management & Low-Power Firmware:

Developed firmware for battery-operated embedded devices with comprehensive power domain management. Implemented peripheral power-on/power-off sequences, managing individual peripheral power states based on system requirements. Configured MCU low-power modes (sleep, deep sleep, standby) with appropriate wake-up interrupt handlers. Implemented clock gating mechanisms to disable peripheral clocks when not in use. Designed power state machines managing transitions between active, idle, and deep sleep states. Achieved measurable reductions in active current consumption, idle current, and standby leakage through firmware-level power optimization.

Technologies: Embedded C, ARM Cortex-M, STM32, power domain control, low-power modes (sleep/deep sleep/standby), clock gating, wake-up interrupts, power state machines

Publications

Citations: 86+

- Alvee, S. R. B., Ahn, B., Kim, T., Su, Y., Youn, Y. W., & Ryu, M. H. (2021). Ransomware attack modeling and artificial intelligence-based ransomware detection for digital substations. *6th IEEE Workshop on the Electronic Grid (eGRID)*, 1–5.
- Su, Y., Ahn, B., Alvee, S. R. B., Kim, T., Choi, J., & Smith, S. C. (2021). Ransomware security threat modeling for photovoltaic systems. *6th IEEE Workshop on the Electronic Grid (eGRID)*, 1–5.

- Alvee, S. R. B., Ahn, B. H., Ahmad, S., Kim, K. T., Kim, T., & Zeng, J. (2022). Device-centric firmware malware detection for smart inverters using deep transfer learning. *IEEE Design Methodologies Conference (DMC)*, 1–5.
- Ahmad, S., Ahn, B. H., Alvee, S. R. B., Trevino, D., Kim, T., Youn, Y. W., & Ryu, M. H. (2022). Advanced Persistent Threat (APT)-style attack modeling and testbed for power transformer diagnosis system in a substation. *IEEE Power & Energy Society Innovative Smart Grid Technologies (ISGT)*.
- Rahman, M. M., Nayeem, M. A., Nahid, S., Alvee, S. R. B., Hasan, R. R., & Rahman, M. A. (2020). On-body humidity sensing antenna with polyimide for BAN applications over 5G networks. *IEEE International IoT, Electronics and Mechatronics Conference (IEMTRONICS)*.
- Alvee, S. R. B. (2022). Study on Artificial Intelligence-Based Ransomware Detection for Digital Substations. *Master's Thesis, Texas A&M University–Kingsville*.